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SEMICONDUCTOR DEVICE AND
METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates in general to a semiconductor device and a method for manufacturing the same, and more particularly to a semiconductor device having a buried conductive layer which is connected to a source/drain of MOS transistor and extends over a gate electrode of the MOS transistor and a method for manufacturing the same.

10 Description of the Related Art

In recent years, as high integration and scale down (shrink) of a semiconductor device have progressed, the alignment margin in the photolithography process for a contact hole which is formed in order to connect a source/drain of a MOS transistor and a wiring layer to each other is being decreased. In addition, the aspect ratio of the contact hole is also being increased. Now, the aspect ratio is defined by the ratio of a depth to a diameter of the contact hole.

20 From the foregoing, the technique is adopted in which the source/drain of the MOS transistor and the wiring layer are not directly connected each other, but are indirectly connected to each other through a buried

conductive layer (an extraction electrode) formed on the source/drain.

Now, the process of manufacturing a MOS transistor employing that barried conductive layer will
5 hereinbelow be described simply with reference to Figs. 1A to 1E.

Firstly, as shown in Fig. 1A, after a field oxide film 102 has been formed in a region to be an isolation region of a silicon substrate 101 by
10 utilizing the well known LOCOS (Local Oxidation of Silicon) method, a gate oxide film 103 is formed in an active region surrounded by the field oxide film 102 by the thermal oxidation method. Thereafter, a poly-crystalline silicon containing phosphorus or arsenic
15 and a silicon oxide film 104 are formed in this order by the CVD method, and those films are then subjected to the anisotropic etching with a photo resist film (not shown), which was formed so as to have a gate electrode pattern by the photolithography technology,
20 as an etching mask, thereby forming a gate electrode 105 formed of that polycrystalline silicon film. In addition, the impurity ions are implanted into the unmasked region with the gate electrode 105 as a mask, thereby forming a pair of lightly doped impurity
25 diffusion layers 106 in surface portions of the silicon substrate 101 on the both sides of the gate electrode.

Next, as shown in Fig. 1B, after a silicon oxide film has been formed on the whole surface of the

silicon substrate 101, the silicon oxide film is selectively etched away by the anisotropic etching, thereby forming a side wall oxide film 107 on each of both side faces of the gate electrode 105 and the
5 silicon oxide film 104 by the anisotropic etching. Incidentally, a portion of the gate oxide film 103 formed on the region which is not covered with the gate electrode 105 or the side wall oxide film 107 is removed concurrently with the selective etching of that
10 silicon oxide film.

Next, as shown in Fig. 1C, a polycrystalline silicon film 108 containing phosphorus or arsenic is formed on the whole surface of the silicon substrate 101 by the CVD method. This polycrystalline silicon
15 film 108 will become a buried conductive layer later. Thereafter, the impurity ions are implanted into the unmasked region with both the gate electrode 105 and the side wall oxide film 107 as a mask, thereby forming a pair of highly doped impurity diffusion layers 109 as
20 a source and a drain in the surface regions of the silicon substrate 101 on the both sides of the gate electrode 105.

Next, as shown in Fig. 1D, after a photo resist film 110 has been applied to the polycrystalline
25 silicon film 108, the photo resist film 110 is processed so as to have a pattern, of the buried conductive layer, having a slit 110a on the gate electrode 105 by the photolithography method. Thereafter, the

polycrystalline silicon film 108 is selectively etched away by the anisotropic dry etching with the photo resist film 110 as an etching mask, thereby processing the polycrystalline silicon film 108 so as to have a pattern which is separated into portions, located on the both sides of the gate electrode 105, with a width of the slit 110a.

Next, as shown in Fig. 1E, the photo resist film 110 is removed. By carrying out the above-mentioned process, it is possible to form buried conductive layers 111, formed of the polycrystalline silicon film 108, which are respectively self-aligned with the pair of impurity diffusion layers 109 of the MOS transistor and each of which extends up to a upper portion of the gate electrode 105.

The buried conductive layers 111 are formed in such a way, whereby the alignment margin of the contact hole for the wiring connection which is formed through the insulating film on the associated buried conductive layer 111 can be increased and also the substantial aspect ratio of that contact hole can be decreased by a thickness of the associated buried conductive layer 111. As a result, it is possible to improve the reliability of the wiring connection in the contact hole portion. In addition, since the impurity diffusion layers 109 each having a shallower junction can also be formed, while suppressing occurrence of any crystal defect in the silicon substrate 101, by the

thermal diffusion from the buried conductive layers 111, formation of the buried conductive layer 111 is also suitable for scale down of the semiconductor device.

5 Now, when forming the above-mentioned buried conductive layer 111, in the process shown in Fig. 1D, the slit 110a of the photo resist film 110 needs to be formed so as to reach the portion above the upper side of the gate electrode 105, and also a width thereof
10 needs to be made much smaller than a width of the gate electrode 105 (a gate length).

 This reason is that if due to the mismatch of alignment in the photolithography process, the central position of the slit of the photo resist film 110 is
15 shifted in the direction of a width of the gate electrode by a distance X as shown in Fig. 2 for example so that the edge of the hole of the photo resist film 110 is located on the associated side wall oxide film 107, and under this condition, the polycrystalline silicon
20 film 108 is subjected to the anisotropic etching, then not only the buried conductive layer 111 in the boundary portion between the buried conductive layer 111 of interest and the associated side wall oxide film 107 will be selectively etched away during the over-
25 etching, but also the thin portion of the side wall oxide film 107 as well as the gate oxide film 103 will be etched away, and finally the surface of the silicon substrate 101 will be exposed.

Then, if the surface of the silicon substrate 101 is exposed, since the etch selectivity of the silicon substrate 101 to the buried conductive layer 111 formed of a polycrystalline silicon film is remarkably small, even the surface of the silicon substrate 101 will be partially etched away, and as a result, a trench 120 will be formed in the silicon substrate 101 by the etching. In such a way, the silicon substrate 101 will be damaged. Such damage of the silicon substrate 101 results in the performance of the MOS transistor being remarkably degraded.

In order to avoid that situation, the width of the slit 110a of the photo resist film 110 needs to be made much smaller than the gate length of the gate electrode 105 so as for the hole edge of the photo resist film 110 not be located on the associated side wall oxide film 107 even if the slight mismatch of alignment occurs. In other words, this means that the gate length of the gate electrode 105 needs to be made much larger than the width of the slit 110a of the photo resist film 110. Thus, even if the width of the slit 110a of the photo resist film 110 should be made a minimum processing size provided by the photolithography technology, the gate length of the gate electrode 105 needs to be made much larger than the minimum processing size. As a result, in the above-mentioned method of forming the buried conductive layer 111, there is a limit in scale down (shrink) of the

transistor.

Now, in order to prevent the damage of the silicon substrate 101 due to the exposure of the surface of the silicon substrate 101, there is considered a method including the step of forming a polycrystalline silicon film, which will form a buried conductive layer later, after further forming an insulating film on the side wall oxide films, or a method including the step of forming a thicker side wall oxide film 107. However, in the former method, by the fine pattern technology, a hole needs to be formed through the insulating film formed on the associated side wall oxide film 107 so that contact is made between the buried conductive layer and the source/drain, and hence the advantage, resulting from the buried conductive layer, of being able to form the buried conductive layer so as to be self-aligned with the source/drain is lost. In addition, in the latter method, the width of each side wall oxide film 107 becomes necessarily large, and hence this results in the fine transistor not being able to be formed. Therefore, the above-mentioned two methods for preventing the damage of the silicon substrate 101 are not suitable for the practical use.

In addition, in JP-A-62-86715, there is described a method for manufacturing a semiconductor device wherein a contact hole is formed so as to be tapered in order to reduce the possibility of

disconnection of the wiring layer.

Now, the manufacturing method described in JP-A-62-86715 will hereinbelow be described simply.

After a contact region having a predetermined pattern has been formed on a semiconductor substrate, an insulating layer is formed so as to cover the contact region. Next, a first photo resist mask is formed which is used to form a first contact hole, and then the insulating layer is etched to the depth of about one half of the thickness of the insulating layer by the anisotropic etching, thereby forming the first contact hole. Thereafter, the first photo resist mask is removed, and then a polycrystalline silicon layer is formed on the whole surface of the semiconductor substrate. Next, the whole surface of the polycrystalline silicon layer is selectively etched away by gas plasma so as to leave a part of the polycrystalline silicon layer on both an edge portion of the first contact hole and a stepped portion of the insulating film. Subsequently, a second photo resist mask is formed which is used to form a second contact hole, and then a second contact hole is formed through the insulating film remaining in the first contact hole by the etching.

While the above-mentioned manufacturing method is suitable for the scale down of the semiconductor device, the etching by which the first contact hole is perforated needs to be stopped at the

time when a thickness of the insulating layer has been halved, and hence the control of the etching amount is difficult to be carried out.

SUMMARY OF THE INVENTION

- 5 In view of the foregoing problems associated with the prior art, an object of the present invention is, in a semiconductor device having a barried conductive layer which is connected to a source/drain of a MOS transistor and which extends over a gate electrode
- 10 of the MOS transistor, to enable a finer transistor as compared with the prior art transistor to be manufactured while preventing a semiconductor substrate from being damaged without complicating the manufacturing process excessively.
- 15 In order to attain the above-mentioned object, according to the present invention, there is provided a method for manufacturing a semiconductor device including the steps of: forming a first insulating film on a semiconductor substrate; forming a
- 20 first conductive film as a gate electrode and a second insulating film on the first insulating film; forming a third insulating film on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film and the second insulating
- 25 film formed thereon; selectively etching away the third insulating film so as to form a side wall insulating film including the third insulating film on each of

both side faces of the first conductive film and the second insulating film and also to expose the semiconductor substrate in portions which are not covered with both the side wall insulating film and the first

5 conductive film; diffusing impurities into the exposed portions of the semiconductor substrate so as to form a source and a drain in the semiconductor substrate; forming a second conductive film to be a part of a buried conductive layer on the whole surface of the

10 semiconductor substrate having the first insulating film, the first conductive film, the second insulating film and the side wall insulating film formed thereon; forming a first mask layer on the second conductive film; processing the first layer so as for the first

15 mask layer to have a pattern which is separated into both side portions with the first conductive film; forming a second mask layer on the whole surface of the semiconductor substrate having the first insulating film, the first conductive film, the second insulating

20 film, the side wall insulating film, the second conductive film and the first mask layer formed thereon; selectively etching away the second mask layer so as to leave a pattern of the second mask layer on each of both side faces of the pattern of the first mask layer;

25 and selectively etching away the second conductive film with the patterns of the first and second mask layers as a mask so as to process the second conductive film into a pattern in which the second conductive film is

separated on the second insulating film.

In addition, according to the present invention, there is provided a semiconductor device including: a semiconductor substrate having a source and a drain of a MOS transistor formed therein; a first insulating film formed on a predetermined region of the semiconductor substrate; a first conductive film as a gate electrode and a second insulating film formed on a predetermined region of the first insulating film; a third insulating film, as a side wall insulating film, formed on each of both side faces of the first conductive film and the second insulating film; a second conductive film connected to one of the source and the drain of the MOS transistor and extending up to a upper portion of the gate electrode of the MOS transistor, the second conductive film having a pattern in which the second conductive film is separated into both side portions with the second insulating film; a first mask layer formed on a first region of the second conductive film; and a second mask layer formed on a second region of the second conductive film along each of side faces of the first mask layer.

Now, after the second conductive film has been selectively etched away so as to be processed into a predetermined pattern, the first mask layer may be removed so that the resultant second conductive film is used as a lower electrode of a capacitor.

According to the present invention, since the

first mask layer is formed on a region of a part of the second conductive film, and the second conductive film is selectively etched away with both the pattern of the first mask layer and the pattern of the second mask layer formed on each of the both side faces thereof as an etching mask, the interval of the patterns of the second conductive films which are adjacent to each other on the second insulating film can be made smaller than that of the patterns of the first mask layers by a width of the pattern of the second mask layer as compared with the interval. As a result, even if the position of the edge portion of the pattern of the first mask layer is slightly shifted, it is possible to reduce the probability that the edge portion of the pattern of the second conductive film is located on the associated side wall insulating film and hence it is possible to promote scale down (shrink) of the semiconductor device.

In addition, when the interval of the patterns of the first mask layers is made a minimum processing size in the photolithography technology, the interval of the patterns of the second mask layers can be made smaller than the minimum processing size. Therefore, the width of the first conductive film, i.e., the gate electrode can be made smaller than that of the prior art, e.g., it can be reduced down to the minimum processing size.

Incidentally, in the present invention, each

of the first and second mask layers may be formed of either a conductive film or an insulating film. In the case where one or both of the first and second mask layer is formed of the conductive film, the mask layer
5 of interest forms, together with the second conductive film, the buried conductive layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects as well as advantages of the present invention will become clear
10 by the following description of the preferred embodiments of the present invention with reference to the accompanying drawings, wherein:

Figs. 1A to 1E are respectively cross sectional views showing a conventional semiconductor
15 device and a method for manufacturing the same in order of process;

Fig. 2 is a cross sectional view useful in explaining the problems associated with the conventional semiconductor device and a method for manufac-
20 turing the same;

Figs. 3A to 3I are respectively cross sectional views showing a semiconductor device according to a first embodiment of the present invention and a method for manufacturing the same in
25 order of process;

Fig. 4 is a cross sectional view showing a structure of one modification of the semiconductor

device according to the first embodiment of the present invention;

Fig. 5 is a cross sectional view showing a structure of another modification of the semiconductor device according to the first embodiment of the present invention; and

Figs. 6A to 6E are respectively cross sectional views showing a semiconductor device according to a second embodiment of the present invention and a method for manufacturing the same in order of process.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The preferred embodiments of the present invention will hereinafter be described in detail with reference to the accompanying drawings.

Referring first to Figs. 3A to 3I, there are illustrated cross sectional views showing a semiconductor device according to a first embodiment of the present invention and a method for manufacturing the same in order of process.

Firstly, as shown in Fig. 3A, a field oxide film 2 with about 400nm thickness is formed in a region to be an isolation region of a P type semiconductor silicon substrate 1 containing boron and having resistivity in the range of 1 to 12 $\Omega \cdot \text{cm}$ by the well known LOCOS method. Thereafter, a gate oxide film 3 with a thickness of 10 to 20nm or so is formed on an active region, which is surrounded by the field oxide

film 2, by the thermal oxidation method.

Then, after a polycrystalline silicon film with about 100nm thickness containing phosphorus or arsenic of 2×10^{20} to 6×10^{20} atoms/cm³ has been formed

5 by the CVD method, a silicon oxide film 4 with about 200nm thickness is formed on that polycrystalline silicon film by the CVD method. Thereafter, a photo resist film (not shown) is applied to the silicon oxide film 4 and then is processed so as to have a gate

10 electrode pattern by utilizing the photolithography technology. Then, the silicon oxide film 4 is selectively etched away with that photo resist film as an etching mask by the anisotropic etching, whereby the silicon oxide film 4 is processed so as to have a gate

15 electrode shape. Subsequently, after the photo resist film has been removed by the ashing, that polycrystalline silicon film is selectively etched away with the silicon oxide film 4 as an etching mask by the anisotropic etching, thereby forming a gate electrode 5

20 formed of that polycrystalline silicon film. In addition, phosphorus ions are implanted into the unmasked region of the P type semiconductor silicon substrate 1 with the gate electrode 5 as a mask at acceleration energy of 30 to 150keV with a dose of $5 \times$

25 10^{12} to 5×10^{13} ions/cm², whereby a pair of lightly doped impurity diffusion layers 6 are formed in the surface portions of the silicon substrate 1 on the both sides of the gate electrode 5.

Next, as shown in Fig. 3B, after a silicon oxide film a thickness of which is in the range of 100 to 200nm or so has been formed on the whole surface of the silicon substrate 1, the silicon oxide film is
5 subjected to the anisotropic etching, whereby a side wall oxide film 7 is formed on each of the both side faces of the gate electrode 5 and the silicon oxide film 4. Incidentally, a part of the gate oxide film 3 in the region which is not covered with the gate elec-
10 trode 5 or the side wall oxide film 7 is removed at the same time that the silicon oxide film is selectively etched away by the anisotropic etching, and as a result, a part of the silicon substrate 1 is exposed. Thereafter, arsenic ions are implanted into the
15 unmasked region of the silicon substrate 1 with both the gate electrode 5 and the side wall oxide film 7 as a mask at acceleration energy of 50 to 100keV with a dose of 5×10^{15} to 5×10^{16} ions/cm², whereby a pair of highly doped impurity diffusion layers 9 as a source
20 and a drain are formed in the surface portions of the silicon substrate 1 on the both sides of the gate electrode 5.

Next, as shown in Fig. 3C, a polycrystalline silicon film 8 containing phosphorus or arsenic and
25 having a thickness in the range of 300 to 500nm or so is formed on the whole surface of the silicon substrate 1 by the CVD method. This polycrystalline silicon film 8 thus formed with become a part of a buried conductive

layer (an extraction electrode) later. Thereafter, a silicon oxide film (a first mask layer) 12 with about 200nm thickness is formed on the whole surface of the polycrystalline silicon film 8 by the CVD method.

5 Next, as shown in Fig. 3D, after a photo resist film 10 has been applied to the whole surface of the silicon oxide film 12, the photo resist film 10 is processed by the photolithography method so as to have a pattern having a slit 10a above the gate electrode 5,
10 the pattern corresponding in a shape to the buried conductive layer. In this connection, a width of the slit 10a of the photo resist film 10 is made substantially the same as a width of the gate electrode (a gate length) 5. Now, if the width of the slit 10a is
15 made to have a minimum processing size in the photolithography technology, then the gate length may also be made substantially the same as the minimum processing size.

 Next, as shown in Fig. 3E, the silicon oxide
20 film 12 is selectively etched away with the photo resist film 10 as an etching mask by the anisotropic dry etching so as to be separated into portions, located on the both sides of the gate electrode 5, with a distance corresponding to the width of the slit 10a.
25 Thereafter, the photo resist film 10 is removed by the ashing.

 Next, as shown in Fig. 3F, a polycrystalline silicon film (a second mask layer) 13 with about 200nm

thickness which will be a part of the buried conductive layer later is formed on the whole surface of the silicon substrate 1 by the CVD method. The thickness of the polycrystalline silicon film 13 is preferably one thirds of a distance between two portions of the silicon oxide film 12 as shown in Fig. 3E so that an area between the two portions is not completely filled up with the polycrystalline silicon film 13.

Next, as shown in Fig. 3G, the polycrystalline silicon film 13 is subjected to the anisotropic dry etching so as to be left only on both the side faces of the silicon oxide film 12.

Subsequently, the polycrystalline silicon film 8 is selectively etched away with both the silicon oxide film 12 and the polycrystalline silicon film 13 as an etching mask, whereby the polycrystalline silicon film 8 is removed except its part underlying both the silicon oxide film 12 and the polycrystalline silicon film 13 so that the polycrystalline silicon film 8 is processed so as to have a pattern which is separated on the silicon oxide film 4. At this time, a separation width of the polycrystalline silicon film 8 is smaller than the width of the slit 10a by a width of the polycrystalline silicon film 13 remaining on both the side faces of the silicon oxide film 12. As a result, the buried conductive layer 11 including the remaining polycrystalline silicon films 8 and 13 is formed.

Next, as shown in Fig. 3H, after a BPSG

(Boro-Phospho Silicate Glass) film 14 a thickness of which is in the range of 500 to 1,000nm or so has been formed on the whole surface of the silicon substrate 1, a photo resist film 15 is applied to the BPSG film 14.

5 Thereafter, the photo resist film 15 is processed by the photolithography technology so as to have a pattern having a hole above the polycrystalline silicon film 8. Then, both the BPSG film 14 and the silicon oxide film 12 are selectively etched away with that photo resist
10 film 15 as an etching mask by the anisotropic etching so as to form a contact hole 16 reaching the polycrystalline silicon film 8.

Next, as shown in Fig. 3I, after the photo resist film 15 has been removed, the heat treatment
15 process for activating the impurity diffusion layers 6 and 9 is carried out and then an aluminum wiring layer 17 is formed which is connected to the polycrystalline silicon film 8 at the bottom of the contact hole 16. Alternatively, a polycrystalline silicon wiring layer
20 17 is formed which is connected to the polycrystalline silicon film 8 at the bottom of the contact hole 16 and then the heat treatment process for activating the impurity diffusion layers 6 and 9 is carried out. Thereafter, the process for forming a passivation film
25 is carried out, whereby a semiconductor device of the present embodiment is completed.

As described above, according to the present embodiment, the separation width of the polycrystalline

silicon film 8 on the silicon oxide film 4 can be made smaller than the width of the slit 10a by the width of the pattern of the polycrystalline silicon film 13 remaining on the both sides of the silicon oxide film 12 since the polycrystalline silicon film 8 is selectively etched away with both the silicon oxide film 12 and the polycrystalline silicon film 13 as the etching mask.

While the first mask layer is formed of the silicon oxide film 12 and also the second mask layer is formed of the polycrystalline silicon film 13 in the present embodiment, the present invention is not limited thereto. That is, it is to be understood that each of the first and second mask layers may be formed of either an insulating film or a conductive film.

In the case where the first mask layer is formed of a conductive layer, a value of a resistance developed between the source/drain of the MOS transistor and the aluminium wiring layer 17 can be reduced since an area of the conductor contacting with the aluminium wiring 17 is increased. In addition, while the contact hole 16 is perforated so as to reach the polycrystalline silicon film 8 in the present embodiment, the present invention is not limited thereto. That is, in the case where the first mask layer is formed of the conductive film, the contact hole 16 may be perforated so as to reach at least the first mask layer.

Since the second mask layer is employed as the etching mask for the polycrystalline silicon film 8 containing the impurities, it has preferably a smaller etching rate than that of the polycrystalline silicon film 8. For example, the second mask layer is preferably formed of a polycrystalline silicon film containing no impurity since the etching rate is increased along with increase of the content of the impurities. In this case as well, the second mask layer will have the electric conductivity due to auto-doping of the impurities from the polycrystalline silicon film 8 containing the impurities. Alternatively, the second mask layer may be formed of an insulating film which has a smaller etching rate than that of the polycrystalline silicon film 8. The structure in this case will be described in detail later.

In addition, while the LOCOS method is employed as the isolation method in the present embodiment, the present invention is not limited thereto. That is, other well known isolation methods such as the field shielding isolation method may also be employed.

Next, the description will hereinbelow be given with respect to a semiconductor device according to a modification of the first embodiment of the present invention with reference to Fig. 4.

Referring to Fig. 4, there is illustrated a cross sectional view showing a structure of an example

which is designed in such a way that one of the source and the drain is connected to a wiring layer 24 through the buried conductive layer 11, and the other is connected to a lower electrode 18 of a capacitor of a
5 DRAM through the buried conductive layer 11.

In order to manufacture a DRAM memory cell as shown in Fig. 4, after a silicon oxide film 22 has been formed on the whole surface of the silicon substrate 1 from the state shown in Fig. 3G, a contact hole is
10 formed through the silicon oxide film 22 so as to reach the polycrystalline silicon film 8, and then the lower electrode 18 formed of a polycrystalline silicon film is formed on the basis of the patterning. Then, after a capacitor dielectric film 19 formed of an ONO film
15 and a upper electrode 20 formed of a polycrystalline silicon film are formed in this order to complete a DRAM capacitor 21, a silicon oxide film 23 is formed on the whole surface of the silicon substrate 1 and then a contact hole is perforated through the silicon oxide
20 film 23. Then, a wiring layer 24 is formed which is connected to the polycrystalline silicon film 8 of the films constituting the buried conductive layer 11.

Referring to Fig. 5, there is illustrated a cross sectional view showing a structure of another
25 modification of the first embodiment which is designed in such a way that one of the source and the drain is connected to a wiring layer 30 through the buried conductive layer 11, and the other is connected to the

buried conductive layer 11 as a lower electrode of a DRAM capacitor.

In order to manufacture a DRAM memory cell as shown in Fig. 5, after a photo resist film has been
5 formed, which has a hole reaching the silicon oxide film 12 formed on one side, from the state shown in Fig. 3G, the silicon oxide film 12 is selectively removed with the photo resist film as an etching mask by the wet etching. Then, the surface of the buried
10 conductive layer 11 is coated with a capacitor dielectric film 26 after removal of the photo resist film, and an upper electrode 27 formed of a polycrystalline silicon film is formed, whereby it is possible to obtain a DRAM capacitor 28 in which the buried
15 conductive layer 11 serves also as a lower electrode. Thereafter, after a silicon oxide film 29 has been formed on the whole surface of the silicon substrate 1, a contact hole is formed through the silicon oxide film 29, and then a wiring layer 30 is formed which is
20 connected to the polycrystalline silicon film 8 on the other side. In this example, the effective surface area of the capacitor is increased and hence the capacity of the capacitor is increased since the polycrystalline silicon film 13 as a projection portion
25 which projects upwardly in the vicinity of the edge portion of the buried conductive layer 11 can be utilized as a part of the lower electrode.

Next, the description will hereinbelow be

given with respect to a semiconductor device according to a second embodiment of the present invention and a method for manufacturing the same with reference to Figs. 6A to 6E.

5 In the manufacturing process of the present embodiment, by carrying out the same process as that shown in Figs. 3A to 3E in the first embodiment of the present invention, there is obtained a structure, as shown in Fig. 6A, having a pattern in which the silicon
10 oxide film (the first mask layer) 12 is separated into portions, located on the both sides of the gate electrode 5, with the width of the gate length.

 Next, as shown in Fig. 6B, a silicon oxide film (a second mask layer) 51 with about 200nm thick-
15 ness is formed on the whole surface of the silicon substrate 1 by the CVD method.

 Next, as shown in Fig. 6C, the silicon oxide film 51 is selectively etched away by the anisotropic dry etching so as to be left only on the both side
20 faces of the silicon oxide film 12.

 Subsequently, the polycrystalline silicon film 8 is selectively etched away with both the silicon oxide films 12 and 51 as an etching mask, whereby the polycrystalline silicon film 8 is selectively removed
25 except its part underlying both the silicon oxide films 12 and 51 so that the polycrystalline silicon film 8 is processed so as to have a pattern in which it is separated on the silicon oxide film 4. At this time,

the separation width of the polycrystalline silicon film 8 is smaller than the width of the slit 10a, which was formed so as to have the same width as the gate length, by the width of the remaining silicon oxide film 51. As a result, the buried conductive layer 11 formed of the remaining polycrystalline silicon film 8 is formed.

Next, as shown in Fig. 6D, after a BPSG film a thickness of which is in the range of 500 to 1,000nm or so has been formed on the whole surface of the silicon substrate 1, a photo resist film 15 is applied to the BPSGA film 14. Thereafter, the photo resist film 15 is processed by the photolithography technology so as to have a pattern having a hole above the buried conductive layer 11. Then, both the BPSG film 14 and the silicon oxide film 12 are selectively etched away with the photo resist film 15 thus processed as an etching mask by the anisotropic etching, thereby forming a contact hole 16 so as to reach the buried conductive layer 11.

Next, as shown in Fig. 6E, after the photo resist film 15 has been removed, the heat treatment for activating both the impurity diffusion layers 6 and 9 is carried out and then an aluminium wiring layer 17 is formed which is connected to the buried conductive layer 11 at the bottom of the contact hole 16. Alternatively, a polycrystalline silicon wiring layer 17 is formed which is connected to the buried conductive

layer 11 at the bottom of the contact hole 16 and then, the heat treatment for activating both the impurity diffusion layers 6 and 9 is carried out. Thereafter, the process for forming a passivation film is carried out, whereby a semiconductor device of the present embodiment is completed.

In the present embodiment as well, similarly to the above-mentioned first embodiment, it is effectively avoided that the surface of the semiconductor substrate is partially etched away while etching the polycrystalline silicon film 8, and the semiconductor substrate is damaged, e.g., a trench is formed in the semiconductor substrate. As a result, the reliability of the MOS transistor can be remarkably improved. In addition, since the separation width of the polycrystalline silicon film 8 can be made smaller than the minimum processing size provided by the photolithography technology, the gate length of the gate electrode 5 can have the minimum processing size and hence the finer MOS transistor can be manufactured.

In addition, since in the present embodiment, the first and second mask layers are respectively formed of the silicon oxide films 12 and 51 each having the etching rate smaller than that of the polycrystalline silicon film 8, the separation width of the polycrystalline silicon film 8 can be made smaller as compared with the case where the second mask layer is formed of a film having a large etching rate.

Incidentally, the present embodiment may also be applied to the method for manufacturing a DRAM in the above-mentioned modifications as shown in Fig. 4 and Fig. 5.

5 Further, while the LOCOS method is employed as the isolation method in the present embodiment, the present invention is not limited thereto. That is, there may be employed other well known isolation methods such as the field shielding isolation method.

10 As set forth hereinabove, according to the present invention, it is possible to reduce a probability that the edge portion of the pattern of the second conductive film is located on the associated side wall insulating film since the separation width of
15 the second conductive film constituting the buried conductive layer can be made smaller than the interval of the patterns of the first mask layers by the width of the pattern of the second mask layer. As a result, it is possible to solve the problem that while etching
20 the second conductive film, even the semiconductor substrate is partially etched away so as to be damaged. As a result, it is possible to remarkably improve the reliability of the MOS transistor without harming the advantage, resulting from the buried conductive layer,
25 that the buried conductive layer can be formed so as to be self-aligned with the source/drain.

 In addition, according to the present invention, the width (the gate length) of the first

conductive film (the gate electrode) can be reduced
down to the minimum processing size since the separation
width of the second conductive film can be smaller
than the minimum processing size. Therefore, it is
5 possible to manufacture the MOS transistor finer than
that by the prior art.

While the present invention has been
particularly shown and described with reference to the
preferred embodiments and the specified modifications
10 thereof, it will be understood that the various changes
and other modifications will occur to those skilled in
the art without departing from the scope and true
spirit of the invention. The scope of the invention is
therefore to be determined solely by the appended
15 claims.